Abstract

The invention relates to a method and related circuitry for multiple phase-splitting. The method includes: while generating M output clocks with a same frequency f1 and different phases, generating N reference clocks with a same frequency (M/N)*f1 and different phases (wherein M>N), and triggering (N/M) frequency division using different periods within each reference clock to generate (M/N) output clocks of different phases for each reference clock, such that the M output clocks of different phases are generated from the N reference clocks of different phases.